A High Power Density Micro-Thermoelectric Generator Fabricated by an Integrated Bottom-Up Approach

Wenhua Zhang, Juekuan Yang, and Dongyan Xu

***Abstract*— In this paper, we report a high power density cross-plane micro-thermoelectric generator (TEG) fabricated by integrating pulsed electroplating with micro-fabrication processes. The TEG consists of a total of 127 pairs of n-type Bi_2Te_3 and p-type Sb_2Te_3 thermoelectric pillars embedded in a SU-8 matrix in order to enhance the overall mechanical strength of the device. Both bottom and top electrical connections are formed by electroplating, which is advantageous because of facile and low cost fabrication and low parasitic electrical resistances. The device demonstrates a maximum power of 2990 μW at a temperature difference of 52.5 K, corresponding to a power density as high as 9.2 mW $\cdot$ cm^{-2}. The power density of our device is more than two times the highest value reported for the electroplated micro-TEGs in the literature, which can be attributed to the low internal resistance and high packing density of thermoelectric pillars. [2015-0348]**

***Index Terms*— Micro-thermoelectric generator, high power density, pulsed electroplating, microfabrication.**

I. INTRODUCTION

THERMOELECTRIC generators (TEGs) are promising for the waste heat recovery in virtue of the ability to directly convert heat to electricity. Despite of their low energy conversion efficiency, TEGs have many advantages including high reliability, long lifetime, and environmental friendliness. Especially, compared to conventional heat engines, TEGs are compact, scalable, and can be easily driven by small temperature differences. Potential applications of TEGs include thermal sensing, thermal management, and thermal energy harvesting to power wireless sensors and microelectronic devices such as wearable medical sensors [1] and wristwatches [2]. TEGs also provide an additional approach to utilize solar energy by first converting it into heat and then recovering heat to generate electricity [3].

Thermoelectric materials have been synthesized via many different approaches, for example, ball milling followed by hot pressing [4], molecular beam epitaxy [5], screen-printing [6], [7], sputtering [8], thermal evaporation [1], and electroplating [9]. In comparison with other techniques, electroplating has advantages of efficient usage of raw materials and compatibility with microfabrication processes [10]. Snyder *et al.* [11] first fabricated a cross-plane micro-thermoelectric device by combining electroplating with microfabrication techniques. In general, cross-plane electroplated micro-TEGs have better performance than in-plane devices because of the high packing density of thermoelectric pillars and a lack of detrimental parasitic heat flow through the substrate [12]. One major challenge in the fabrication process of cross-plane micro-TEGs lies in forming electrical connections between n-type and p-type thermoelectric pillars, especially top connectors. To date, two methods have been demonstrated for fabricating top connectors: electroplating and flip-chip bonding. Snyder *et al*. formed top connectors on free-standing thermoelectric pillars by electroplating [11]. Glatz *et al*. [13] used a negative SU-8 photoresist as the supporting mold for the TEG; and top connectors were fabricated by electroplating and etching on the flipped photoresist mold that was released from the substrate. Kim and Oh [14] adopted flip-chip bonding technique to fabricate top connectors and they observed an internal resistance of 3.7 kΩ for a thin-film TEG, which is attributed to the large interfacial resistance of flip-chip joints. Recently, Roth *et al*. [15] developed several micro-TEGs with different combinations of n-type and p-type materials including Bi_2Te_3/Cu, annealed Bi_2Te_3/Cu, and Bi_2Te_3/Sb_xTe_y by electroplating. They also adopted flip-chip bonding technique to form top connectors and an internal resistance of $\sim$134 Ω is observed for their Bi_2Te_3/Sb_xTe_y TEG. The internal resistance of a TEG consists of electrical resistances of both n-type and p-type thermoelectric pillars and electrical resistances of top and bottom connectors (including interfacial electrical resistance between connectors and pillars). For a fixed temperature difference, the open-circuit voltage (V_{oc}) of the TEG is fixed. The maximum power (P_{max}) can be achieved when the internal resistance of the TEG (R_{in}) and the load resistance are matched, which can be estimated by

$$P_{max} = \frac{V_{oc}^2}{4R_{in}}. \quad (1)$$

A large parasitic electrical resistance will dramatically reduce P_{max} that a TEG can deliver. Therefore, the electrical resistances of connectors and electrical contact resistance should be minimized in order to achieve a large power output.

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In this work, we developed a cross-plane micro-TEG with 127 pairs of n-type Bi_2Te_3 and p-type Sb_2Te_3 thermoelectric pillars by a bottom-up approach integrating electroplating with microfabrication processes. All the key components of the TEG including bottom connectors, both n-type and p-type thermoelectric pillars, and top connectors are fabricated by electroplating. The micro-TEG we developed shows a very low internal resistance (~13 Ω), presumably due to the low electrical resistivity of thermoelectric materials and the low parasitic electrical resistance of the electroplated connectors. A maximum power density of 9.2 mW cm^{-2} is achieved for our TEG at a temperature difference of 52.5 K, which is more than two times the highest value reported so far for the electroplated micro-TEGs in the literature [15].

II. Thermoelectric Materials

In this work, Bi_2Te_3 and Sb_2Te_3 are chosen as n-type and p-type thermoelectric materials for the TEG, respectively, which are synthesized by pulsed electroplating in a three-electrode setup using a potentiostat (Princeton Applied Research, VersaSTAT 3F). The effect of deposition parameters on the composition, microstructure, and thermoelectric properties of the electroplated Bi_2Te_3 films has been systematically investigated and the details can be found in our previous publication [10]. For Bi_2Te_3, an aqueous electrolyte containing 30 mM Bi^{3+}, 40 mM $HTeO_2^+$, and 1.7 M HNO_3 is used for the deposition. A pulse-on potential (E_{on}) of 0 mV vs. Ag/AgCl (saturated KCl) and a pulse-off potential (E_{off}) of 200 mV are fixed to achieve stoichiometric composition. Pulse-on time (t_{on}) and pulse-off time (t_{off}) are set as 0.1 s and 2.5 s, respectively, for obtaining dense and compact microstructure. The Seebeck coefficient is determined to be -63 μV K^{-1} at room temperature for the Bi_2Te_3 films electroplated under the same condition [10].

In comparison with Bi_2Te_3, it is more challenging to deposit Sb_2Te_3 by pulse electroplating, presumably due to the difficulty to achieve the stoichiometric composition. This is attributed to the small binding energy of Sb_2Te_3 by Schumacher *et al*. [16], which leads to the strong dependency of the composition on the deposition potential. The aqueous electrolyte for the deposition of Sb_2Te_3 is prepared by dissolving Sb_2O_3 and TeO_2 powders (Alfa Aesar, 99.99%) in nitric acid with tartaric acid complex agent. The final clarified electrolyte contains 5.6 mM $[Sb_2(C_4H_4O_6)^2]^{2+}$, 10 mM $HTeO_2^+$, 1.0 M HNO_3, and 0.84 M tartaric acid. The deposition parameters are set as $E_{on} = -250$ mV, $E_{off} = 43$ mV, $t_{on} = 0.1$ s, and $t_{off} = 2.5$ s. The in-plane Seebeck coefficient of the as-deposited Sb_2Te_3 thin films is measured by using a home-made setup at room temperature. Fig. 1 shows the scanning curves of thermoelectric voltage vs. temperature difference for heating and cooling processes, both of which show a linear dependence and overlap with each other. The Seebeck coefficient of Sb_2Te_3 can be extracted from the slope of the linear fitting curve and is found to be 116 μV/K at 300 K.

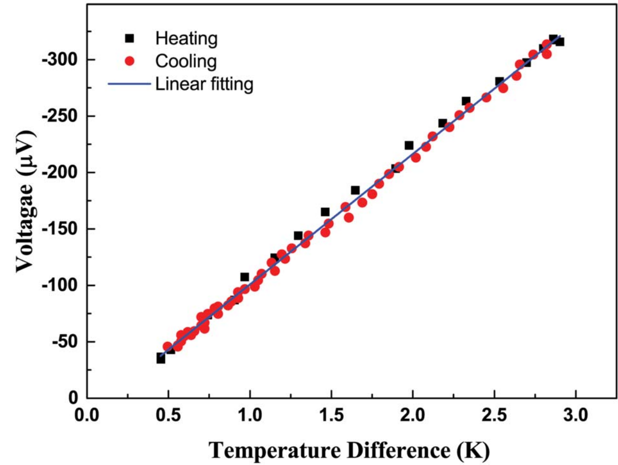

Fig. 1. The induced thermoelectric voltage vs. temperature difference for the electroplated Sb_2Te_3 at room temperature. The Seebeck coefficient determined from the slope of the linear fitting curve is 116 μV/K.

III. Device Fabrication

The schematic of the fabrication process for the micro-TEG is shown in Fig. 2. The fabrication starts with a 500 μm silicon (Si) wafer with 300 nm thermal oxidation layer on both sides. The wafer is first cleaved into 14 mm × 14 mm square chips as the substrate of the micro-TEG. The oxidation layer prevents the electrical current leakage through the substrate. Then, both sides of the substrate are coated with 50 nm chrome (Cr) and 100 nm gold (Au) layers by sputtering. During the process, the sidewalls of the substrate are also coated with Cr/Au layers, which are important for forming electrodes for electroplating as discussed below. Next, bottom connectors and thin connecting lines are patterned by wet etching using photoresist as a mask. It is worth noting that Au and Cr layers on sidewalls and bottom surface of the substrate are protected by photoresist during the etching process. As a result, each bottom connector is connected with bottom surface of the substrate through a thin Cr/Au connecting line and the Cr/Au layers on the sidewalls, which will work as the electrode for electroplating. In addition, two large Cr/Au pads are also fabricated on the substrate during this step as electrodes for connecting with testing instrument or external circuits, which are not shown in Fig. 2(a) for clarity but can be seen from the optical image of the final micro-TEG in Fig. 2(k). The sputtered Cr/Au layers demonstrate a large electrical resistance due to small thickness and possible increase of resistivity caused by the diffusion between two metals [17]. It is very costly and time consuming to deposit thick Au layer by sputtering. Therefore, in order to reduce the total electrical resistance, one more step of photolithography is performed and bottom connectors and two large contacting pads are thickened by depositing 1.5 μm Au layer via DC electroplating due to its low cost and high deposition rate, as shown in Fig. 2(a).

In the next step, a 10 μm thick SU-8 layer is fabricated by photolithography with two 200 μm open holes patterned on each bottom connector (Fig. 2(b)). Two open holes serve as the mold for depositing n-type and p-type thermoelectric materials, respectively. In addition, we also fabricate pinholes with a diameter of 60 μm in the SU-8 layer, close to those 200 μm open holes, as shown in Fig. 3. These pinholes are designed to prevent mechanical damage to thermoelectric pillars which might occur during the heating process due to

(a) (e) (i)

(b) (f) (j)

(c) (g) (k)

(d) (h)

2.5 mm

Fig. 2. The schematic of the bottom-up fabrication process for the micro-TEG. (a) Cr/Au bottom connectors and contacting pads are patterned by sputtering and wet etching. The Au layer is thickened by electroplating to reduce electrical resistance. (b) A permanent SU-8 mold with open holes is patterned for the deposition of thermoelectric materials. (c) A thin layer of photoresist is patterned to cover one group of holes and n-type Bi_2Te_3 is deposited in the selectively opened holes by the pulse electroplating. (d) The deposited n-type Bi_2Te_3 is covered by photoresist and p-type Sb_2Te_3 is deposited in the remaining holes. (e), (f), (g) Top connectors are patterned on the lapped top surface. (h) 3 μm Ni is deposited by DC electroplating as top connectors. (i), (j) After removing the photoresist, Cr/Au layers on the sidewalls and backside of the substrate are etched away. The fabricated micro-TEG is bonded with the top cover for testing. (k) Top view of the fabricated micro-TEG before bonding with the top cover.

the mismatch of coefficients of thermal expansion between thermoelectric materials and SU-8. The SU-8 mold is cured at 150 °C for 15 min and turned into a permanent mold to enhance the mechanical strength of the micro-TEG. It should be noted that the temperature applied to the hot side of the TEG should be lower than the hard bake temperature of the SU-8 mold (150 °C). The drawback of the SU-8 mold is that it allows the parasitic heat loss across the TEG. Then, a thin layer of photoresist with a thickness of 1-2 μm is coated on the SU-8 mold by spin coating. Next, one set of holes are opened by photolithography and the whole chip is etched in oxygen plasma at 50 W for 1 min to remove organic residues on the exposed Au surface in open holes. N-type Bi_2Te_3 is deposited in open holes by the pulse electroplating as shown in Fig. 2(c). The deposition condition is given in section II. In this step, all the n-type thermoelectric pillars are deposited concurrently under the same condition since all the bottom connectors are connected together. The desired thickness can be achieved for the electroplated Bi_2Te_3 by controlling the number of pulse cycles. After the deposition of n-type materials, the thin photoresist layer is removed in acetone. Then, another layer of photoresist is used to cover the deposited n-type materials and p-type Sb_2Te_3 is deposited in the rest of open holes by pulsed electroplating as shown in Fig. 2(d).

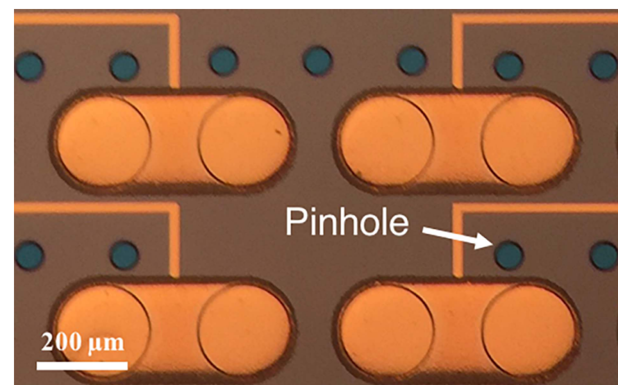

Fig. 3. Pinholes with a diameter of 60 μm are fabricated in the SU-8 layer, close to those 200 μm open holes, to release thermal stress.

As mentioned above, one critical step for the fabrication of the micro-TEG is to form the top connectors which connect all thermoelectric pillars electrically in series. During the

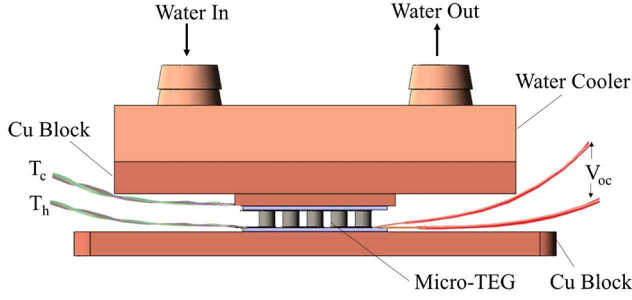

Fig. 4. The schematic of the testing setup.

pulsed electroplating, we intentionally make n-type and p-type thermoelectric pillars thicker than the SU-8 mold. A lapping process is adopted to make the top surface even. In this step, the top surface of the chip is placed against a rotating textile fabric surface for roughly 10 min. 0.05 μm de-agglomerated alumina suspension (Allied High Tech Products, Inc.) is used as the abrasive. Then, top connectors are formed by electroplating in a temporary photoresist mold on the lapped top surface of the permanent SU-8 mold with embedded thermoelectric pillars, as shown in Fig. 2(e)-(i). A thin photoresist layer is first patterned with shaped holes for the deposition of top connectors (Fig. 2(e)). A 100 nm Au layer is sputtered on the entire top surface, serving as the seed layer for electroplating (Fig. 2(f)). A second photoresist layer is then patterned, which has the exactly same pattern as the first layer (Fig. 2(g)). Two photoresist layers are well aligned with each other and serve as the mold for the deposition of top connectors. A 3 μm thick low-stress nickel (Ni) layer is deposited by DC electroplating (Fig. 2(h)). After that, the chip is soaked in acetone to remove the temporary photoresist mold. Next, Cr/Au layers on the sidewalls and backside of the substrate and partial connecting lines are chemically etched away to break external electrical connections among bottom connectors. All thermoelectric pillars are electrically connected in series by bottom and top connectors. Before bonding with the top cover, a thin layer of thermal grease is spread onto the active device area to reduce interfacial thermal resistance. Then, a Si chip with thermal oxidation layer is pressed and glued to the SU-8 mold around the edge with a thin layer of thermal grease in between. The schematic of the final micro-TEG is shown in Fig. 2(j).

IV. Device Characterization

Fig. 2(k) shows the optical image of the prototype micro-TEG before bonding with the top cover. The micro-TEG consists of 127 pairs of n-type Bi_2Te_3 and p-type Sb_2Te_3 thermoelectric pillars. Each pillar has a diameter of 200 μm and a thickness of $\sim$10 μm. The effective device area (A_e) covered by thermoelectric pillars in the center is around 0.65×0.5 cm^2. A homemade testing setup (Fig. 4) is used to characterize the performance of the micro-TEG. The device is mounted on a rectangular ceramic board with copper (Cu) conducting lines and electrodes. Two large Cr/Au pads on the micro-TEG are electrically connected with Cu electrodes on the testing board by wire bonding. Two Type K thermocouples are tightly attached to the substrate and top cover of the micro-TEG by thermally conductive paste to measure temperatures at hot side (T_h) and cold side (T_c), respectively. The micro-TEG is sandwiched by a designed Cu fixture, as shown in Fig. 4, for the testing. The assembled testing setup is heated from the bottom by a hot plate with the PID control. The setup is cooled on the top side by an open-loop cooling water system. T_h, T_c, and the generated V_{oc} are recorded by a digital multimeter (Agilent, 34401A).

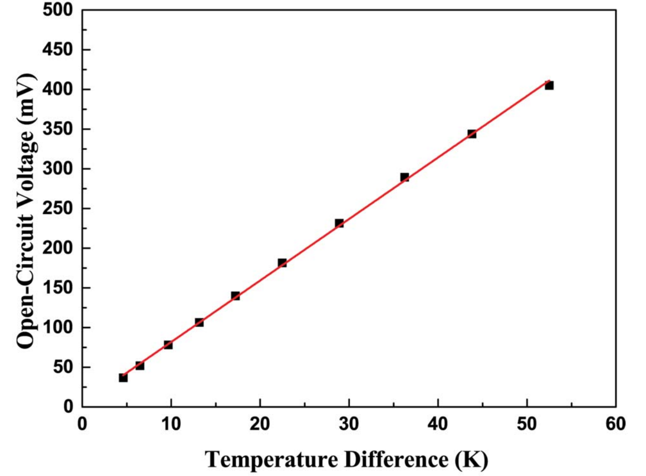

Fig. 5. The measured open-circuit voltage vs. temperature difference.

The testing is carried out for temperature differences from 4.6 K to 52.5 K. For each data point in Fig. 5, V_{oc} is recorded after the temperature difference cross the micro-TEG reaches the steady state. The measured V_{oc} demonstrates a liner dependence on temperature difference and the experimental data can be fitted by

$$V_{oc} = 7.7\Delta T + 4.3[\mathrm{mV}], \tag{2}$$

with high accuracy ($R^2 = 0.9993$). The highest V_{oc} obtained in the measured temperature range is 405 mV at the temperature difference of 52.5 K. The open-circuit voltage per unit temperature difference for the micro-TEG is determined to be 7.7 mV/K, which is much lower than the value directly estimated from Seebeck coefficients of Bi_2Te_3 and Sb_2Te_3 ($(63 + 116)\ \mu\mathrm{V/K} \cdot 127 = 22.7$ mV/K). The large performance drop is mainly due to the fact that the actual temperature difference across thermoelectric pillars is much smaller than the temperature difference we recorded for the device. As shown in Fig. 4, two thermocouples, used to measure T_h and T_c, are mounted on top surfaces of the substrate and the top cover, respectively. A large portion of the temperature drop is across the top cover structure of the micro-TEG. The interfacial thermal resistances at bottom and top connectors might also cause a certain temperature drop. From the measured and the ideal open-circuit voltages per unit temperature difference, we can estimate that the effective temperature difference for our micro-TEG is approximately 34% of the measured temperature difference.

In addition to V_{oc}, one important parameter for the micro-TEG is P_{max} at a certain temperature difference. To determine P_{max}, the micro-TEG is connected with a 100 Ω potentiometer, which serves as the external load. The load voltage (V) and current (I) are measured by a digital multimeter

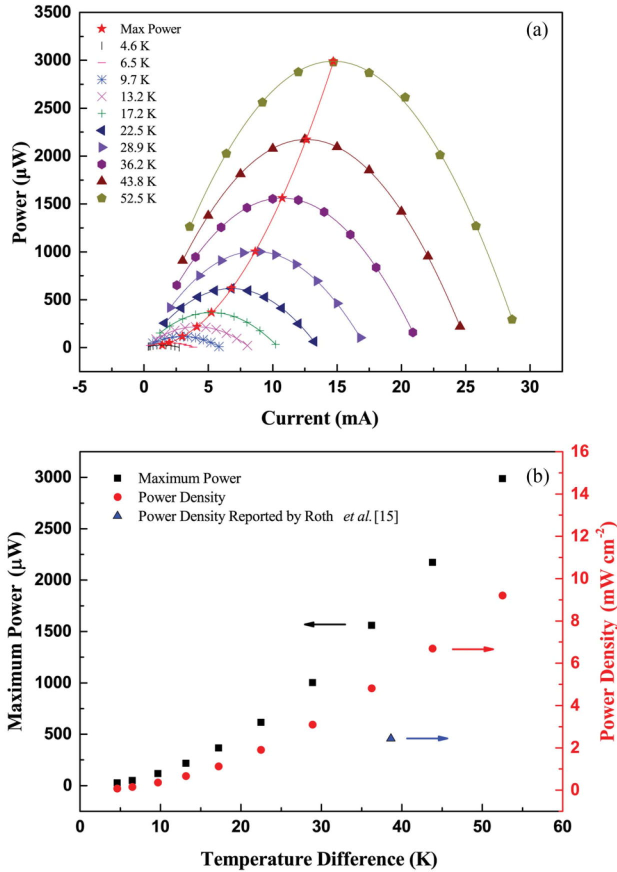

Fig. 6. (a) The calculated power vs. the recorded current at different temperature differences. The maximum power is denoted as the red stars. Solid lines are the polynomial fitting curves. (b) The maximum power and power density at different temperature differences. The power density of our device is more than two times the highest value reported so far for the electroplated micro-TEGs [15].

(Agilent, 34401A) and a source meter (Keithley, 2425). At each temperature difference, V and I are recorded when the potentiometer is gradually adjusted from 10 Ω to 100 Ω. For each load resistance, the power output can be calculated from the recorded V and I. Fig. 6(a) plots the calculated power as a function of the current for temperature differences ranging from 4.6 K to 52.5 K. The solid line represents the polynomial fitting curve at each temperature difference. P_{max} and the corresponding current (I_m) are determined and plotted as red stars and the polynomial fitting curve is shown as the red line. Fig. 6(b) shows P_{max} at different temperature differences. A maximum power of 2990 μW is obtained at a temperature difference of 52.5 K, corresponding to an effective power density (P_{max}/A_e) of 9.2 mW cm^{-2}. For the electroplated micro-TEGs, the maximum power density reported so far is 2.4 mW cm^{-2} at a temperature difference of 38.6 K for the annealed Bi_2Te_3/Cu TEG developed by Roth *et al.* [15]. For the same temperature difference, our micro-TEG generates a maximum power of 1711 μW, corresponding to a power density of 5.3 mW cm^{-2}, which is more than two times the best value reported by Roth *et al.* [15]. Compared to the Bi_2Te_3/Sb_xTe_y TEG in Roth *et al.*'s work [15], our TEG produces a 40 times larger power density, which can be attributed to the low internal resistance of the TEG and high

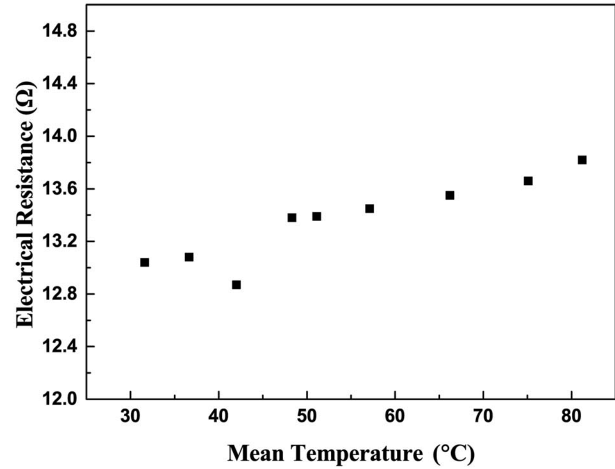

Fig. 7. The internal resistance of the micro-TEG as a function of the mean temperature.

packing density of thermoelectric pillars. R_{in} of our micro-TEG can be calculated by

$$R_{in} = R_{load} = P_{max}/I_m^2, \quad (3)$$

where R_{load} is the load resistance when the power output reaches the maximum value. R_{in} is shown in Fig. 7 as a function of the mean temperature when temperature difference across the micro-TEG is changed from 4.6 K to 52.5 K. For the whole measurement temperature range, R_{in} slightly increases from 13 Ω to 13.8 Ω. The Bi_2Te_3/Sb_xTe_y generator developed by Roth *et al.* [15] consists of 71 pairs of thermoelectric pillars with a diameter of 300 μm and a thickness up to 135 μm, which demonstrates an electrical resistance of 134 Ω. The electrical resistance per pair of thermoelectric pillars for their device is 1.9 Ω. Our TEG is composed of 127 pairs of thermoelectric pillars and has an internal resistance of 13 Ω. The electrical resistance per pair of thermoelectric pillars is calculated to be 0.1 Ω. Our thermoelectric pillars have a diameter of 200 μm and a thickness of 10 μm. Assuming that electrical properties of thermoelectric materials remain constant for different dimensions, if we make our thermoelectric pillars with the same dimensions as Roth *et al.*'s, electrical resistance per pair of thermoelectric pillars will be around 0.6 Ω, which is still substantially lower than that of Roth *et al.*'s Bi_2Te_3/Sb_xTe_y TEG [15]. The lower electrical resistance of our TEG is presumably due to the low electrical resistivity of thermoelectric materials and the low contact resistance of electroplated connections. Electroplated coatings are commonly used for reducing contact resistance in commercial electrical contact applications [18]. For the thermoelectric-pillar/metal interface made by the soldering process, the electrical contact resistivity has been reported to be typically between 10^{-9} and 10^{-8} Ωm^2 [19]. A recent work measured the electrical contact resistivity between plated Au and Bi_2Te_3/Sb_2Te_3 to be between 10^{-11} and 10^{-10} Ωm^2 [20], which is more than one order of magnitude lower than that of the soldered interface. On the other hand, the high packing density of thermoelectric pillars also contributes to the high power density of our TEG. We integrated 127 pairs of thermoelectric pillars in an area of 0.65 × 0.5 cm^2,

while Roth *et al.* fabricated 71 pairs of thermoelectric pillars in an area of 0.98×0.98 cm^2 [15]. The packing density of our TEG is about 5.3 times that of the TEG developed by Roth *et al.* [15].

It has been shown in the literature that thermal annealing treatment can enhance thermoelectric properties of the electroplated Bi_2Te_3 and Sb_2Te_3 [15], [16], [21]. In our current fabrication process, we did not intentionally anneal the deposited thermoelectric materials. We expect that the power density of our TEG can be further enhanced if thermal annealing treatment is adopted in the fabrication process.

V. Conclusion

In this work, we developed a cross-plane micro-TEG via a bottom-up approach combining the pulsed electroplating and microfabrication processes. All the key components of the TEG including bottom connectors, both n-type and p-type thermoelectric pillars, and top connectors are fabricated by electroplating. The micro-TEG we developed demonstrates a very low internal resistance ($\sim$13 Ω), presumably due to the low electrical resistivity of thermoelectric materials and the low parasitic electrical resistance of the electroplated connectors. A maximum power density of 9.2 mW cm^{-2} is achieved at a temperature difference of 52.5 K, which is the highest value reported so far for the electroplated micro-TEGs. The high power density of our TEG can be attributed to the low internal resistance of the TEG and high packing density of thermoelectric pillars. Our study demonstrates that electroplating is beneficial for forming electrical connectors of the micro-TEG due to facile and low-cost fabrication and low parasitic electrical resistance. The high power density micro-TEG we developed can be potentially used to harvest low-grade waste heat that naturally exists in buildings to power wireless sensor network. It could also provide power for wearable electronic devices by converting body heat into electricity.

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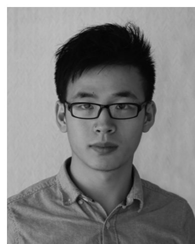

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